**Lab Report: 2**



**Digital System Design Lab**

**Spring 2023**

**Submitted by:**

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**Semester: 6**

“On my honor, as a student of University of Engineering and Technology Peshawar, I have neither nor received unauthorized assistance on this academic work”

**Submitted to:**

**Eng:Muhammad Usman**

# Introduction To Xilinx Ise and S3board Objectives

Objective of this Lab are

* Introduction to FPGA
* Xilinx

# FPGA

FPGAs are programmable digital logic circuits. It can be programmed to do almost any digital function. There are at least 5 companies making FPGAs in the world. Xilinx is the biggest name in the FPGA world.

The FPGA kits available in our labs are SPARTAN-6 STARTER KIT BOARD.

# XILINX

The Integrated Software Environment (ISE™) is the Xilinx® design software suite that allows us to take our design from design entry through Xilinx device programming. The ISE Project Navigator manages and processes your design through the following steps in the ISE design flow.

##  Design Entry

Design entry is the first step in the ISE design flow. During design entry, we will create source files based on our design objectives.We can create your top-level design file using a Hardware Description Language (HDL), such as VHDL, Verilog, or ABEL, or using a schematic.

##  Synthesis

After design entry and optional simulation, we run synthesis. During this step, VHDL, Verilog, or any language designs become netlist files that are accepted as input to the implementation step.

##  Implementation

After synthesis, we run design implementation, which converts the logical design into a physical file format that can be downloaded to the selected target device.

##  Verification

We can verify the functionality of your design at several points in the design flow. We can use simulator software to verify the functionality and timing of your design or a portion of your design. The simulator interprets VHDL or Verilog code into circuit functionality and displays logical results of the described HDL to determine correct circuit operation.

##  Device Configuration

After generating a programming file, we configure our device. During configuration, we will generate configuration files and download the programming files from a host computer to a Xilinx device.

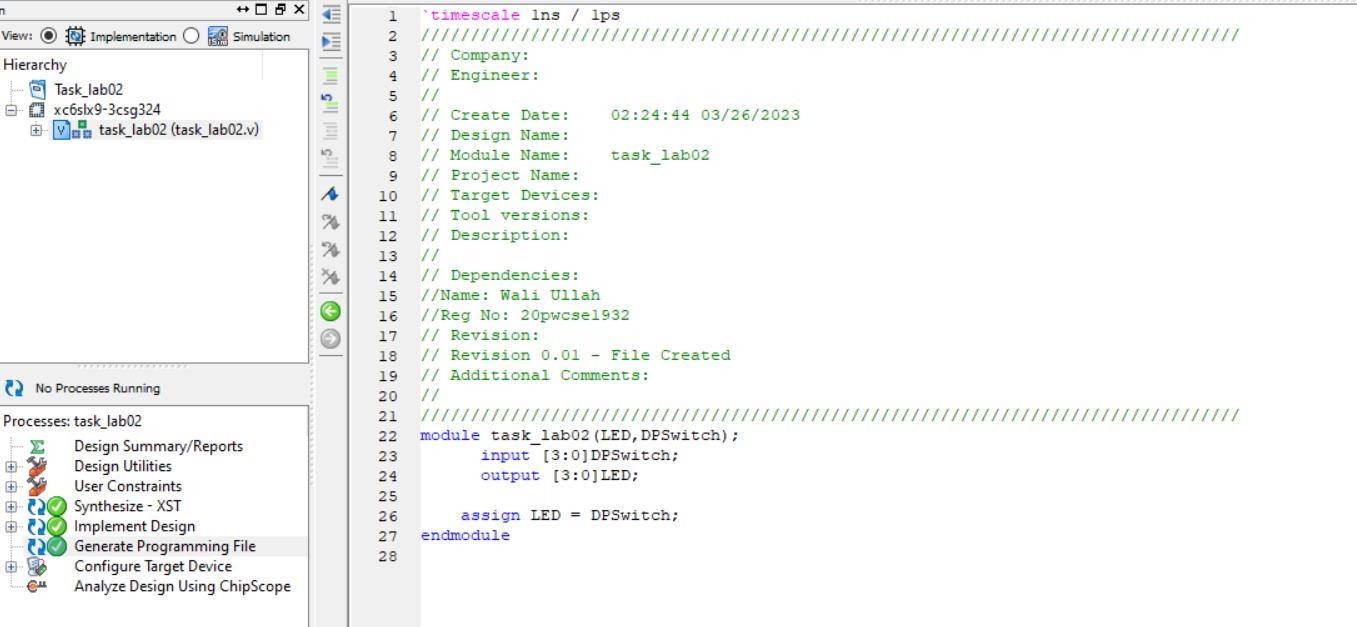
The code can be synthesized by the following steps.

1. First of all the USER DEFINED CONSTRAINT file is created and added in the Project
2. Code is then synthesized.
3. Design is implemented.
4. Programming file is then generated which can be downloaded into the FPGA.

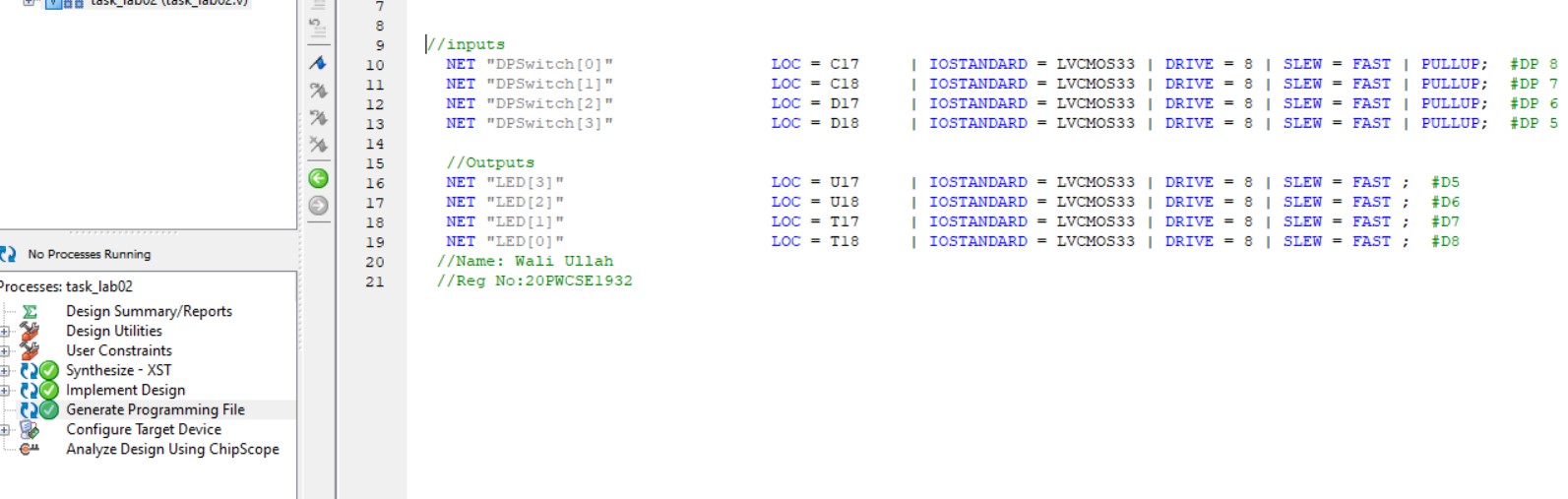
**Task 01**

Develop a program to control on Board LED using On board available switch

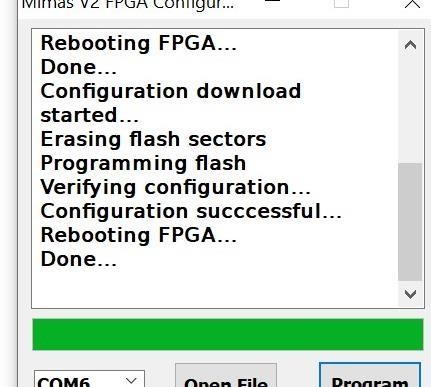
## Verilog Code



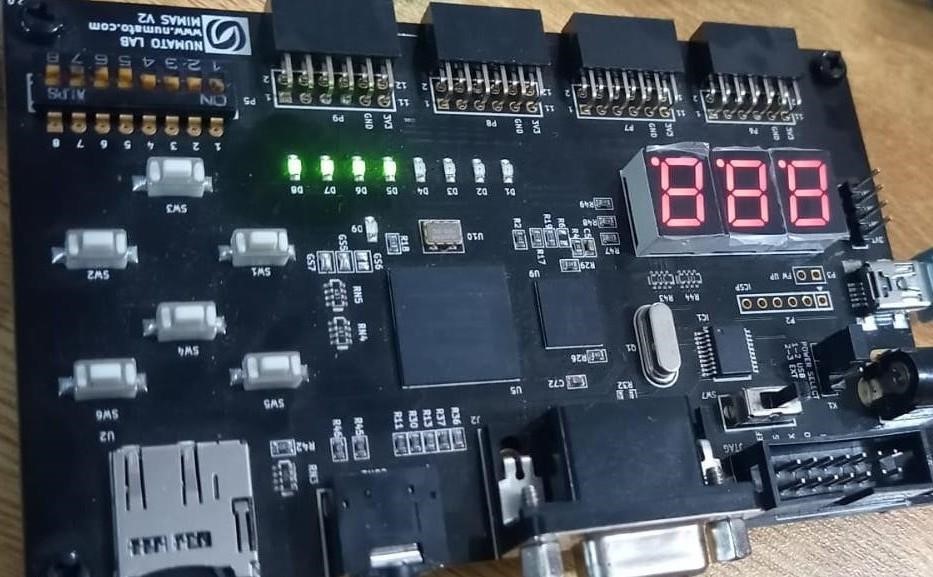
## Design Implementation



## Configuration



## Output

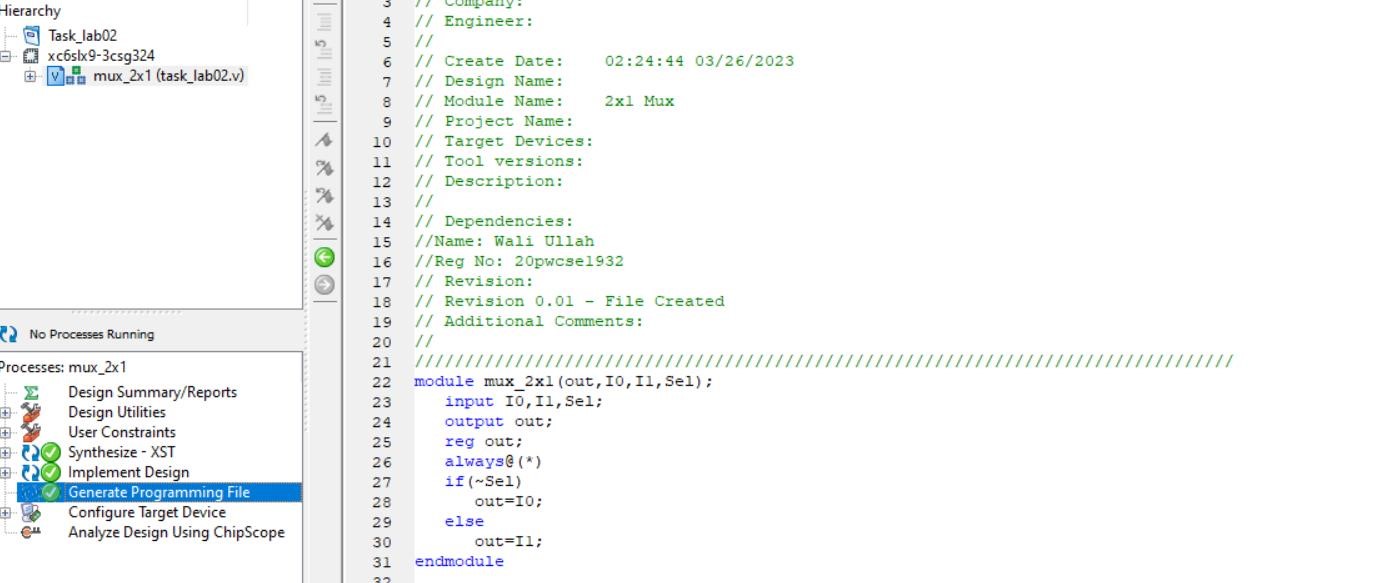


## Task 02

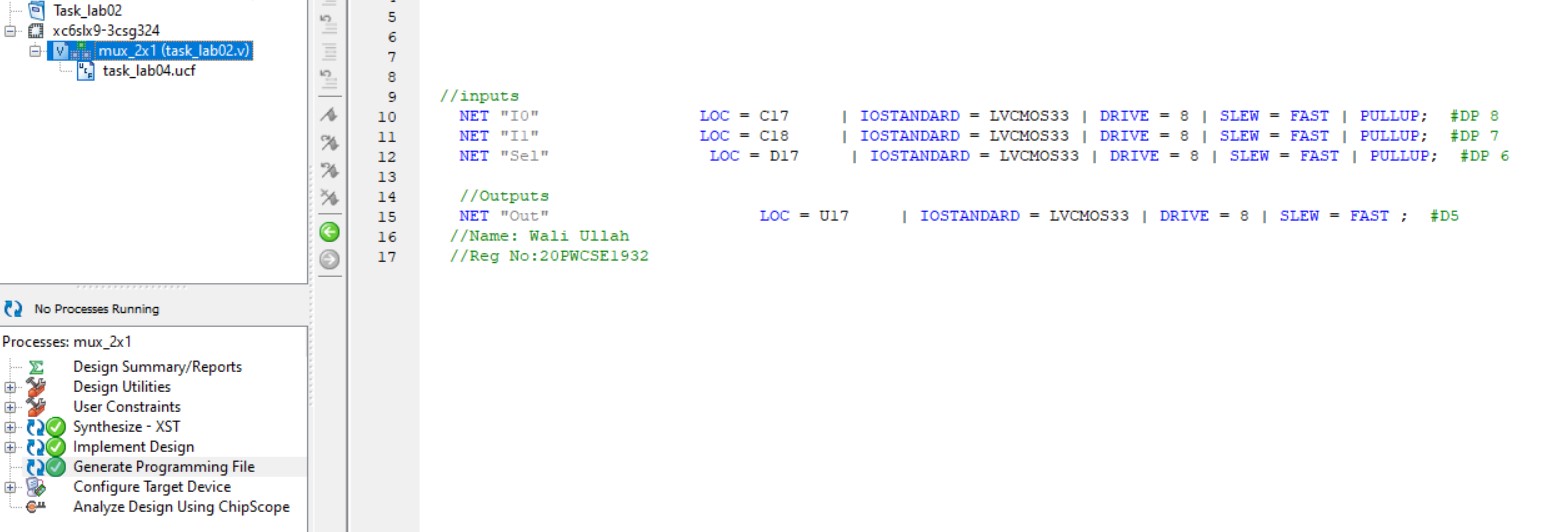
Develop a program that implements a 2x1 multiplexer on the board. Connect the inputs to switches and output to led. View the Synthesized Circuit and the Maximum Combinational path delay (Critical path).

## Code

## 



## Design Implementation



## Output

